

In the Specification:

Please amend paragraph 20 as follows:

[20] The solution idea underlying an aspect of the present invention is to provide a sole input/output interface capable of performing both functions of the serial and parallel type, but with a reduced pin number. Essentially, the parallel operation modes are emulated by the serial interface.

Please delete paragraph 21 as follows:

~~**[21]** On the basis of this solution idea, the technical problem is solved by an architecture as previously described and defined in the characterizing part of claim 1 attached.~~

Please amend paragraph 48 as follows:

[48] A second block **5** "Instruction Decoder" receives a signal from the least or less significant pin ADD_PAD<0> of the address pin group and it is in charge of decoding in the SPI serial mode the several protocol commands. This block **5** receives the information by the sole input pin ADD_PAD<0> of the address pins.

Please amend paragraph 49 as follows:

[49] A third block ~~**6-7**~~ "Addlatched<23:0>" comprises a plurality of latch registers, preferably twenty-four registers, necessary for the temporary storage of the addresses ADD_PAD<10:0>.

Please amend paragraph 50 as follows:

[50] A fourth block ~~**7-6**~~ "Data<7:0>" comprises in turn a group of latch registers, particularly eight registers, and it serves to store temporarily the input and output data on the pins DATA_PAD<7:0>.